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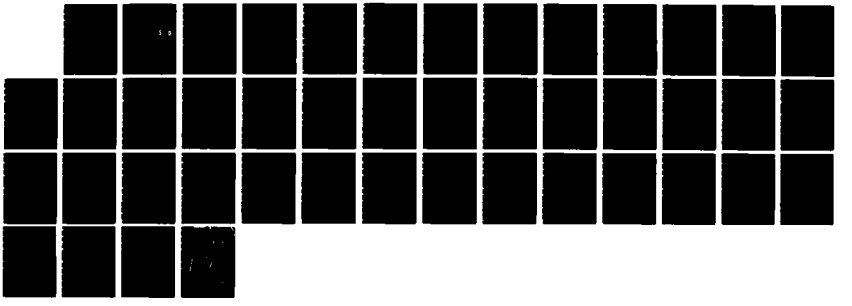

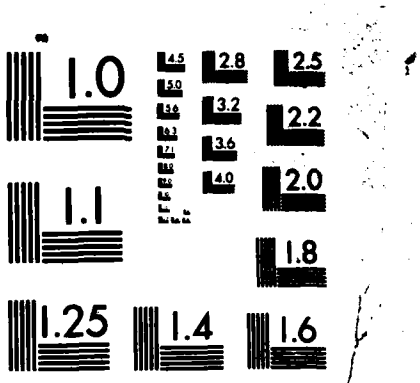

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THE GENERATION OF FIELD SENSITIVE INTERFACE STATES IN COMMERCIAL CMOS DEVICES

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31 May 1984

Technical Report

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The introduction of metastable interface states by the application of a voltage stress has been studied in MOS devices from eleven commerical CMOS processes. Field sensitive interface effects have been observed in samples from four out of five Al metal gate processes but only one out of six Si gate processes. A square root field dependence of the interface state generation has been observed. The initial interface state density has been characterized using a low temperature C-V displacement method and the results correlated to the radiation hardness of the oxides.

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SECTION 1
INTRODUCTION

The degradation of silicon MOS devices by ionizing radiation is a well known and extensively studied phenomenon. The interest in this subject is sustained by the need to produce even more radiation hard microelectronic circuits for use in systems subjected to nuclear and space radiation environments. Research in this area has sought to understand the basic mechanisms responsible for hole trapping and interface state buildup following irradiation in order to adjust IC manufacturing processes and improve circuit hardness. Efforts in this area have sought a means of examining the nature and behavior of defects responsible for hole trapping and interface state buildup in a nondestructive manner prior to device irradiation. Previously published work [1], Appendix A, on the generation of field-sensitive interface states has demonstrated that a neutral defect present at the $Si\text{-}SiO_2$ interface can be observed in a nondestructive reversible manner using a combination of high temperature voltage stressing and low-temperature C-V measurements. A model for these defects was proposed [2], Appendix B, that accounts for the time, temperature, and field behavior of these defects as well as being consistent with existing data in the literature on the buildup of interface states caused by ionizing radiation or charge injection. Further work on the relationship between the amount of defects present before irradiation and the flat band voltage shift, ΔV_{FB}, of a series of laboratory prepared MOS capacitors [3] suggested a strong correlation with oxide radiation hardness.

The purpose of the present study is to apply the techniques developed for the observation of field sensitive interface states to a large number of commercially available CMOS products that represent a broad range of process parameters. The selection of this sample matrix allows for certain generalizations regarding the experimental results which have not been possible in other studies using samples from a single laboratory or

fabrication line. On the other hand, the use of commercial parts does not allow for the systematic variation of any one process parameter that may control or affect the observed phenomenon and therefore this one study cannot hope to characterize the physics involved in the experimental observations.

SECTION 2
EXPERIMENTAL

2.1 EXPERIMENTAL DESCRIPTION

A complete description of the experimental technique for measuring field sensitive interface states is given in [1] and [2]. The measurement of the amount of field-sensitive interface states is basically the difference between high frequency C-V curves measured at 77 K where one curve represents the unstressed interface and the second curve is for the sample voltage-stressed at some temperature above 77 K (most typically 300 K). It should be emphasized, once again, that this observed phenomenon differs from interface states introduced through bias-temperature-stress experiments in that the states are introduced reversibly and can be allowed to relax out in times less than it took to introduce them.

2.2 SAMPLE MATRIX

The sample matrix for this study consists of p- and n-type MOS capacitors that are included in the test structures contained on process control monitor (PCM) chips. The PCMs were obtained from four manufacturers and represent eleven different CMOS processes that produce commercially available CMOS integrated circuits. Some details of the different processes are listed in Table I. There are five Al metal gate processes and six Si gate processes represented. Of the five metal gate processes, three (B1, C2, and C3) are described by their manufacturers as radiation hardened processes. One Si gate processes (D2) is offered as a radiation hardened process. Gate oxide thicknesses range from 55 nm to 140 nm.

The sample matrix was characterized by high frequency (100 kHz) and quasistatic CV measurements made at 300 K to determine the initial interface state density D_{IT} and flat band voltage V_{FB}. It was also characterized by

Table 1. CMOS processes.

Manufacturer	Process	Gate Technology	Oxide Thickness (Å)	Area (10^{-3} cm^2)	Field-Sensitive States (p-type only)	D_{IT} (10^{10} cm^{-2}-eV^{-1})		Sample Size (No. of Devices)	
						p-type	n-type	p-type	n-type
A	1	Si	1400	0.65	Y	1.2	0.9	9	7
B	1*	Al	650	0.18	Y	2.0	1.3	9	8
	2	Al	1000	3.23	N	4.0	2.5	9	6
	3	Si	650	2.33	N	0.3	0.8	8	--
	4	Si	650	8.10	N	1.3	3.3	7	10
C	1	Al	1050	0.65	Y	1.0	0.8	4	5
	2*	Al	750	0.65	Y	2.5	2.4	4	5
	3*	Al	800	0.65	Y	2.1	2.3	6	7
D	1	Si	550	0.46	N	1.2	1.0	7	5
	2*	Si	550	0.46	N	2.9	2.4	8	2
	3	Si	850	0.46	N	1.6	0.7	4	5

*Rad hard process

high-frequency CV measurements made at 77 K by the conventional method to determine the shape of the unstressed C-V curve and by the Jenq [4] technique to again look at the initial interface state density. The Jenq technique measures the difference between a C-V curve measured from accumulation to depletion and one in which the MOS capacitor was inverted with light energy while being held in deep depletion and then measured from that inverted voltage to accumulation. Following the initial characterization, the sample matrix was surveyed to determine which devices exhibited the phenomenon of field sensitive interface states. For this determination, all devices were biased with a field of +3 MV/cm (positive with respect to the gate) at 300 K for 30 min. They were then cooled to 77 K with the field applied. At 77 K, the field was removed and a high-frequency C-V measurement was made. The stressed and unstressed C-V curves were compared to determine the effect of field sensitive interface states. Where differences between the two curves were observed, the samples were returned to 300 K and allowed to relax unbiased. After a short time at 300 K, they were returned to 77 K and an additional high-frequency C-V measurement was made to confirm that the effect of the 300 K bias was indeed reversible.

Those devices that exhibited field sensitive interface states were further characterized to determine the field, temperature, and time dependence of the bias voltage on the magnitude of the field sensitive interface state effect.

Lastly, the devices were irradiated in a Co^{60} source while under a +1 MV/cm bias to determine if a correlation between the field-sensitive interface state phenomenon and the radiation hardness of these commercial oxides could be observed. The samples were maintained under bias until the C-V measurement could be performed. Elapsed time between the end of the irradiation and the measurement was approximately 1 h.

SECTION 3
RESULTS AND DISCUSSION

The results of the initial interface state determination are shown in Table I. The interface state densities range from 3×10^9 cm^{-2} eV^{-1} to 4×10^{10} which shows that all devices are of reasonable quality and there is nothing in this measurement to distinguish one from another. The results of the initial survey for field-sensitive interface states are also shown in Table I. Of the eleven CMOS processes that were studied, five displayed the field-sensitive interface phenomenon and six did not. Of the five processes that displayed the phenomenon, all but one were aluminum gate CMOS. Process A-1 which did show the effect of reversibly induced interface states is the only silicon gate process to do so.

Both n- and p-type capacitors were measured in this study, but only the p-type capacitors (*p-well technology*) displayed the phenomenon. The C-V curves exhibiting field-sensitive interface state behavior for the five processes are shown in Fig. 1.

Of the six processes which did not display field-sensitive interface states, all were silicon gate technologies except for B-2 which was an Al metal gate CMOS technology. The existence of the field-sensitive interface states appears to favor the metal gate processing technologies where the gate oxidation temperature and other processing temperatures tend to be higher. Si-gate process A-1 with the thickest gate oxide of any capacitor measured also has a relatively high gate oxidation temperature (>950°C) which may account for it appearing with the rest of the metal gate device. However, the absence of field-sensitive interface states from metal gate process B-2 which also has a relatively high gate oxidation temperature remains an impediment to concluding that field-sensitive interface states are related in a straightforward manner to gate technology or gate oxidation temperature.

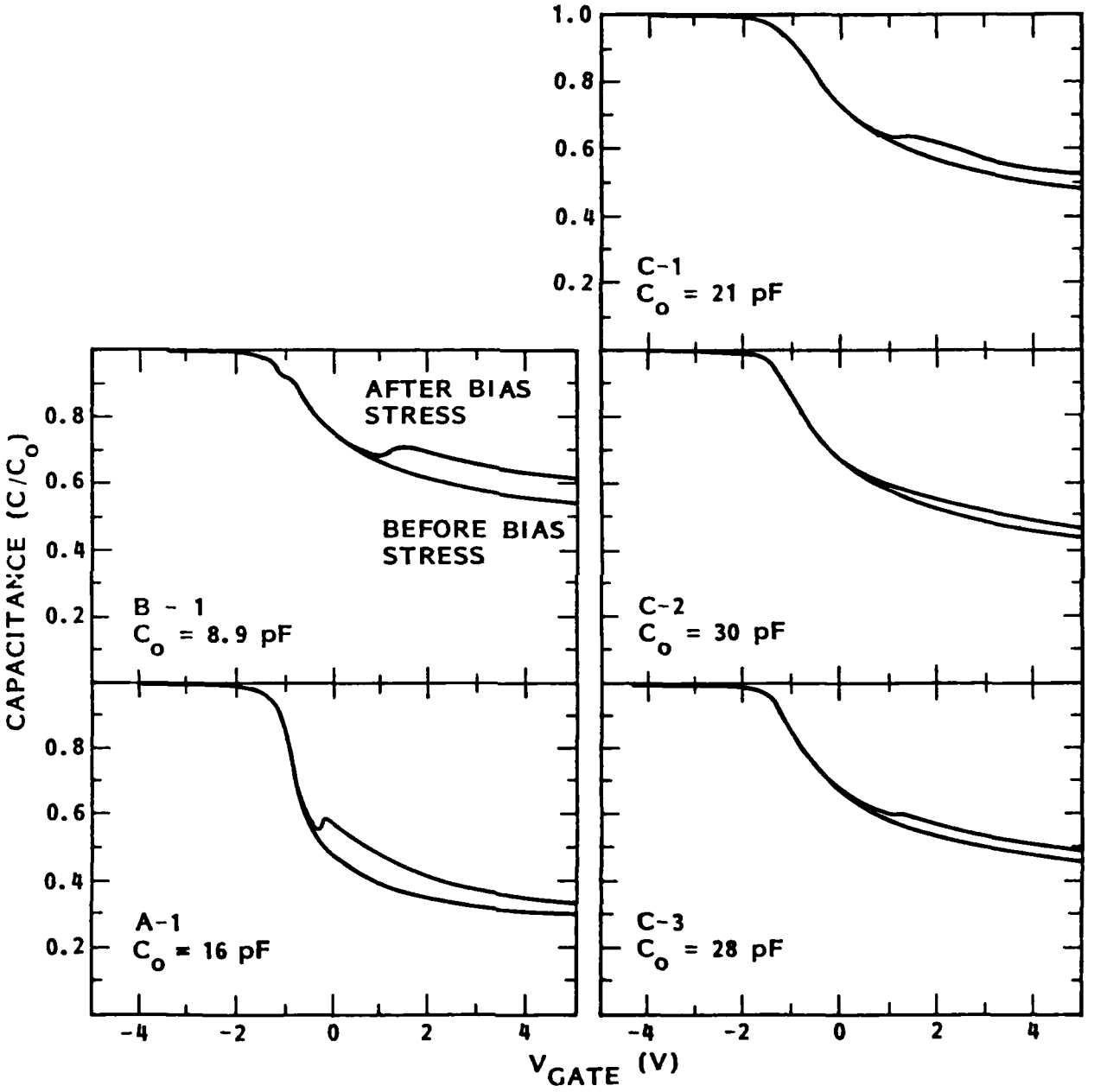

Figure 1. C-V response measured at T = 77 K for five CMOS processes before and after bias stress at 3 MV/cm, 30 min, 300 K. This shows the presence of field sensitive states.

The five processes that exhibited field-sensitive interface states were subjected to further tests to determine if the magnitude of the field-induced difference between the stressed and unstressed C-V curves had a time, temperature, or field dependence. A complete time, temperature, and field parametric study has not been attempted at this time because of the large effort required. Instead, a survey of the sample matrix was performed to establish trends. Figure 2 shows the results of bias stress tests performed on samples from process C-1. The devices were biased with positive voltage on the gate at 300 K for 10 min with varying electric fields. The difference (ΔV) between the stressed and unstressed C-V curves measured at 77 K is plotted as a function of bias field. The slope of the curve in Fig. 2 is 1/2 showing a square-root dependence on electric field for the amount of field sensitive interface states. Other processes displayed a very weak or no field dependence. Work reported earlier[1,2] on n-type capacitors showed a square root field dependence for negative bias and a linear dependence for positive bias. The cause of the different electric field dependence of the number of field sensitive interface states observed in the current samples under test is not understood, but it is possibly a result of different oxide structures which would be characteristic of the individual device processing histories. Further investigation of this field dependence, including the effect of negative gate bias on the field sensitive interface states, would provide more guidance in this matter but was not possible to do within the scope of this contract.

Initial characterization of the sample matrix included a measurement of the unstressed capacitor at 77 K in the manner detailed by Jenq[4]. The results of the light-assisted C-V measurements are shown in Figs. 3 and 4. A curve for process B-3 is not shown as it was very similar to B-4. The rationale for grouping the curves in Figs. 3 and 4 is that all curves in Fig. 4 display a unique and distinct response to the measurement technique employed. That response is the long portion of the inversion-to-accumulation curve that is parallel to the original depletion curve which is an indication of deep lying traps at the interface. The curves in Fig. 4 also represent the four processes that are described by the manufacturers as radiation hardened.

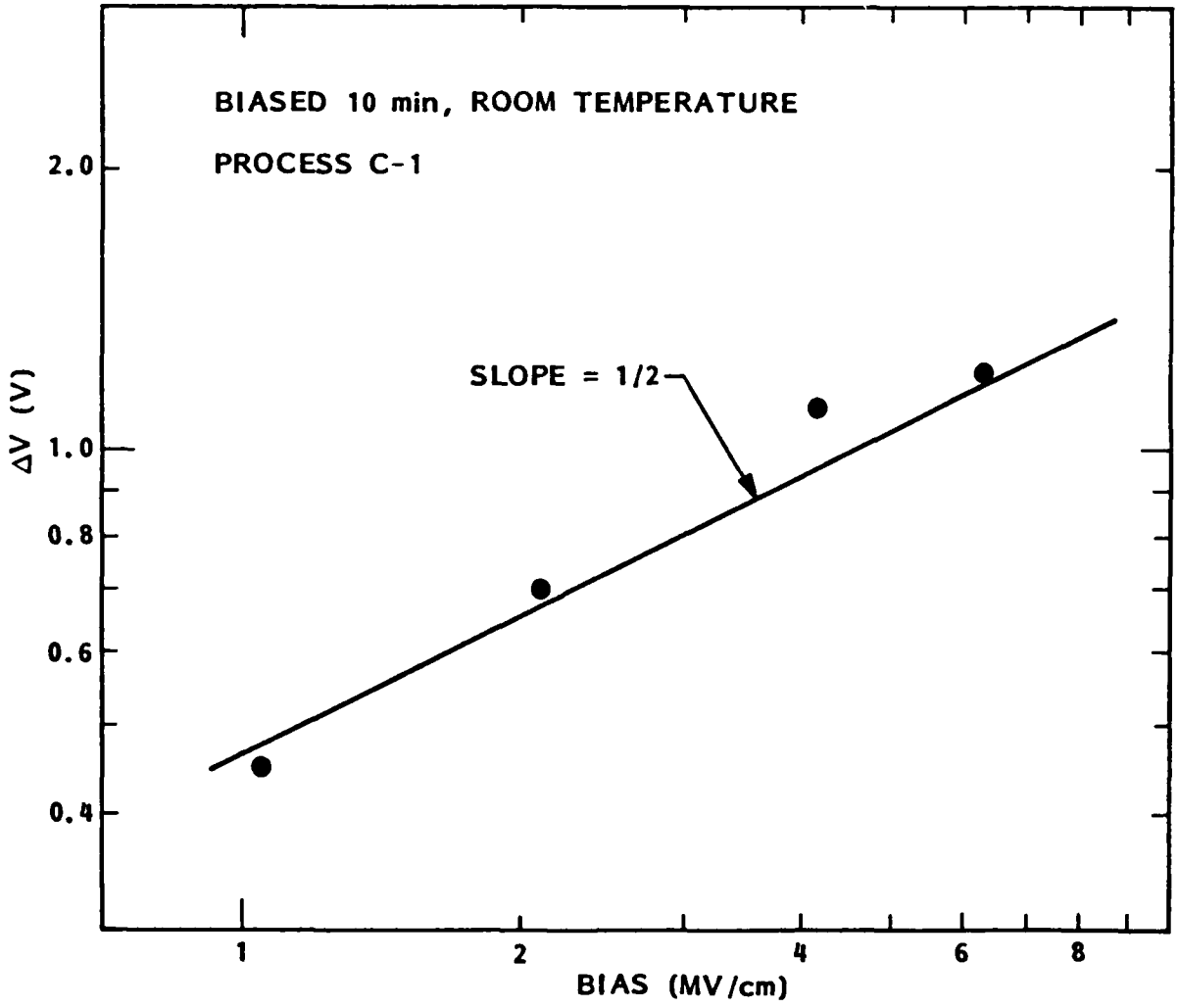

Figure 2. Voltage shift due to field sensitive states as a function of bias electric field for process C-1.

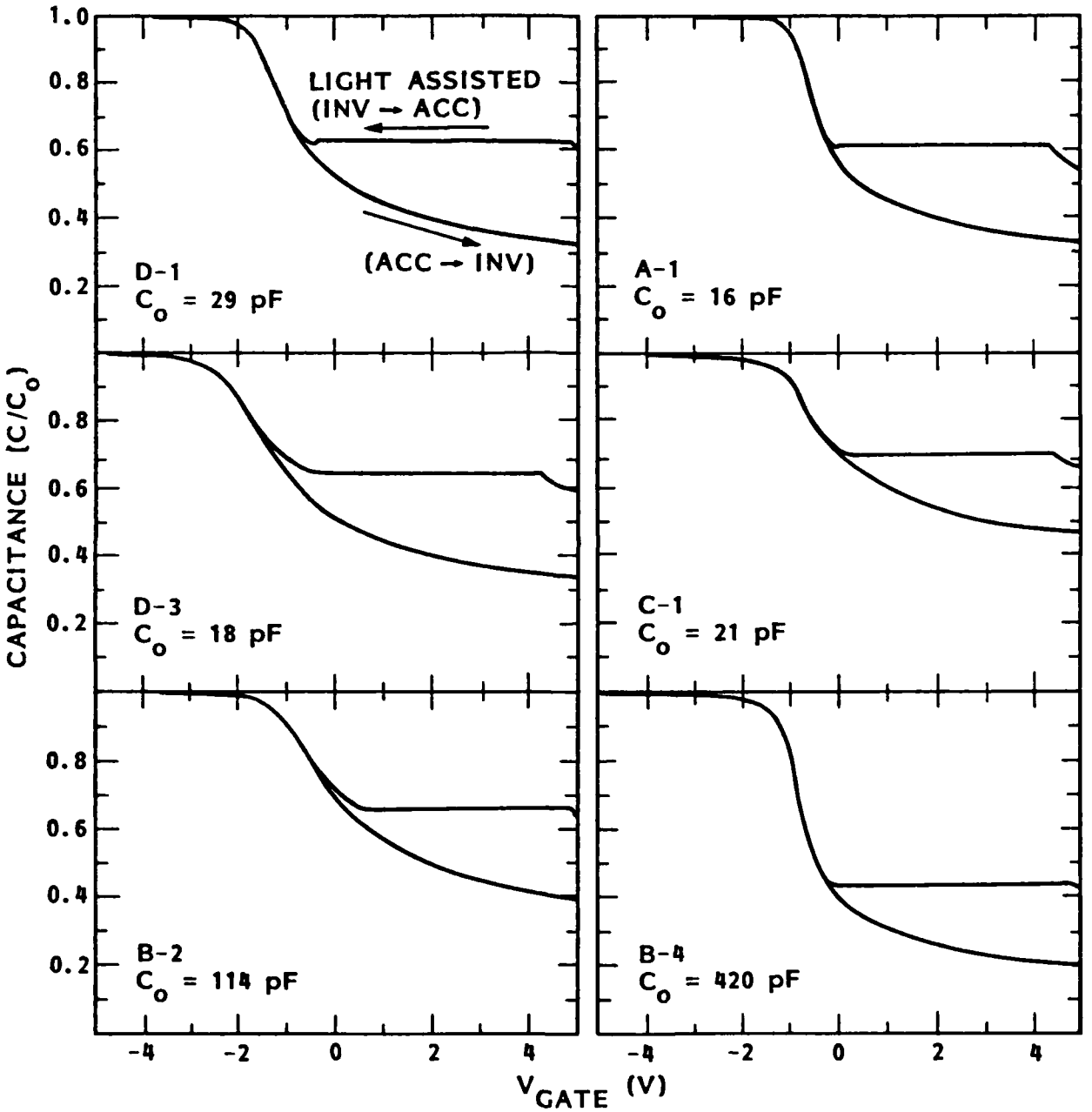

Figure 3. C-V response measured at T = 77 K using the Jenq technique for the nonradiation hard process lines.

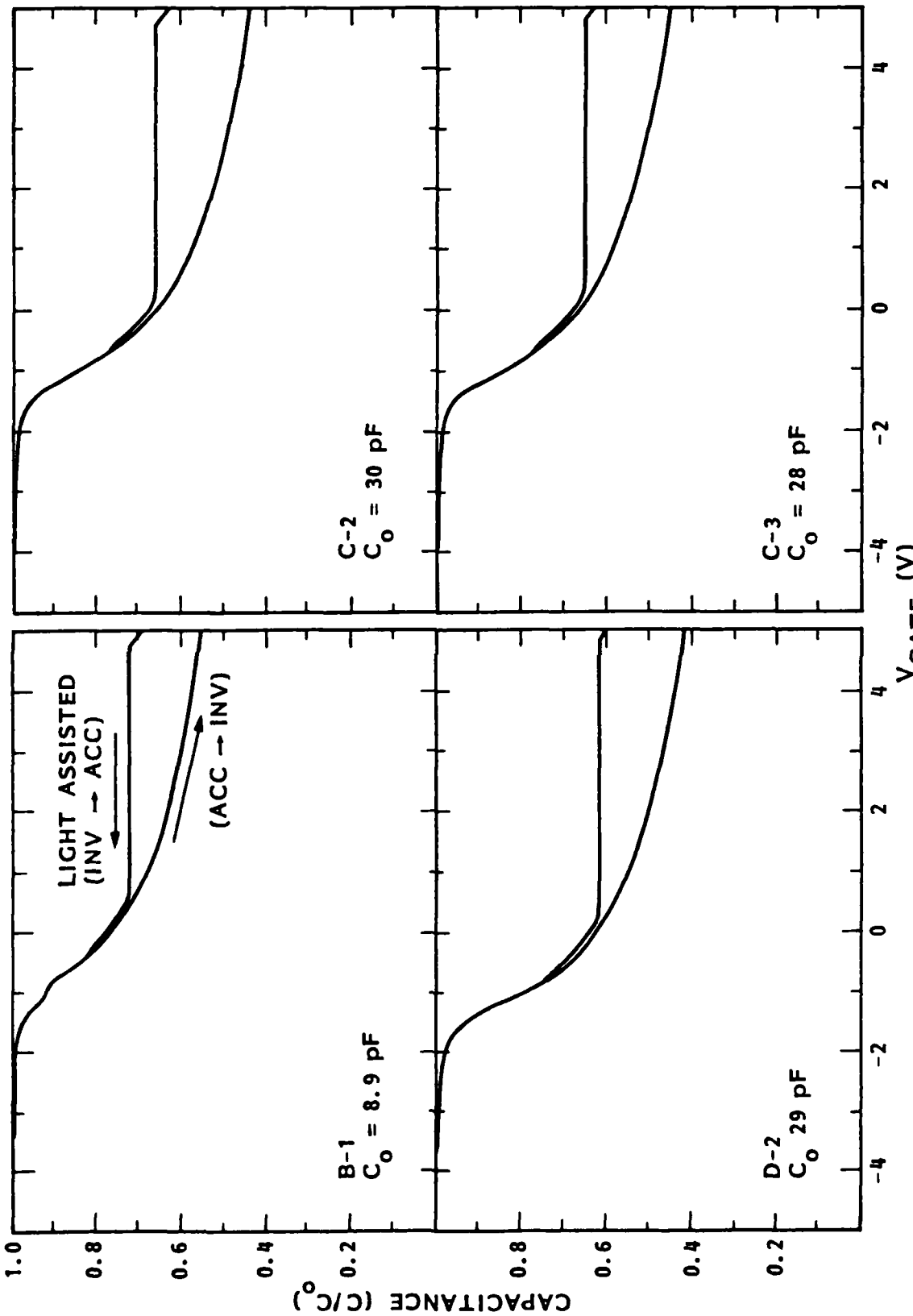

Figure 4. C-V response measured at T = 77 K using the Jenq technique for the radiation hard process lines.

To complete this experimental survey of the eleven commericial CMOS processes, the samples where irradiated in a Co^{60} source at doses of 10^4, 10^5, and 10^6 rads (Si). In Fig. 5, the radiation-induced flat band voltage shifts for the n-type MOS capacitors are plotted as a function of total dose. Due to the very large sample size, soft devices were not irradiated at 10^6 rads (Si) and devices which were described as hard were not irradiated at 10^4. The flat-band voltage shifts as a function of total dose for the p-type MOS capacitors are shown in Fig. 6. The data in Figs. 5 and 6 confirm the manufacturer's designation. Processes B-1, C-2, C-3, and D-2 are harder than the rest with B-1 showing less than 0.2-V flat-band shift at 10^6 rads (Si) for the n-type capacitors and approximately 1.6-V flat-band shift for the p-type capacitors.

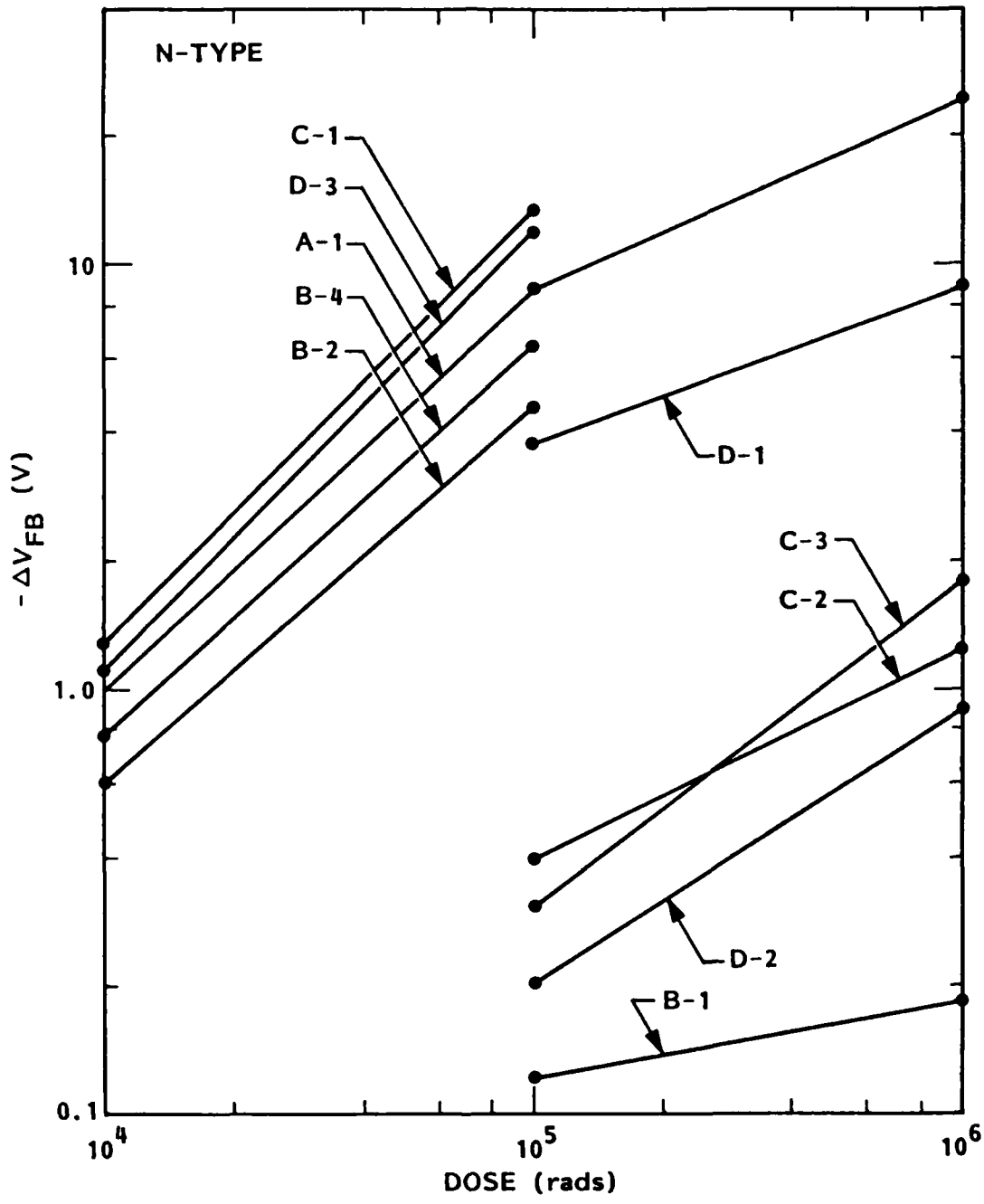

Figure 5. Measured flatband voltage shift for the n-type devices due to Co^{60} gamma irradiation.

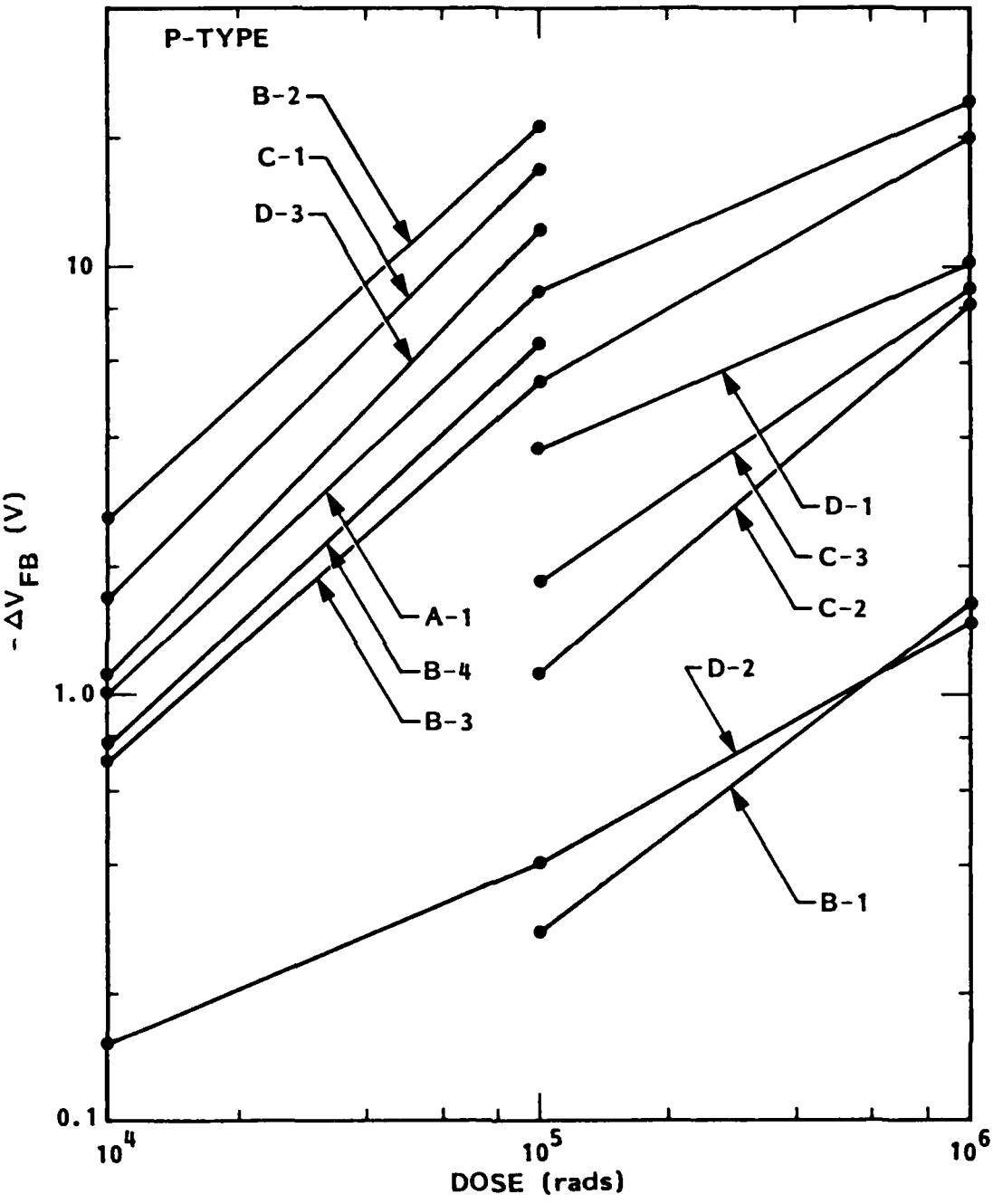

Figure 6. Measured flatband voltage shift for the p-type devices due to Co^{60} gamma irradiation.

SECTION 4
CONCLUSIONS

A sample matrix consisting of n- and p-type MOS capacitors on process monitor control chips from 11 commercially available CMOS lines has been electrically characterized to determine if any of them exhibit the phenomenon of field sensitive interface states. Five of the 11 displayed the reversible field sensitive interface state phenomenon, four metal gate and one Si gate process. These results indicate that the defect accounting for the phenomenon has a complicated origin but is perhaps associated with high-temperature processing. In addition, no correlation between the existence of field sensitive interface states and oxide radiation hardness was observed. Thus, field sensitive states are not directly related to radiation hardness from process to process, but to relative hardness within a process.[1,2]

Characterization of the interface of unstressed capacitors using the Jenq technique revealed that the hard devices responded with a unique inversion-to-accumulation curve indicative of deep electron traps at the interface. The nature of this unique response and its apparent correlation to radiation hardness are not currently understood. Further work is necessary to establish whether or not it is a real correlation.

The designation of "hardened" devices by the manufacturer was confirmed in radiation tests.

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APPENDIX A

GENERATION OF FIELD-SENSITIVE INTERFACE STATES

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We have observed the generation of interface states in SiO_2 metal oxide semiconductor (MOS) capacitators that are field- and time-dependent as well as thermally activated. A strong correlation has been found between these metastable interface states and the radiation hardness of the MOS devices. The number of interface states generated is linearly dependent on the applied field with a threshold field for occurrence. There is a $t^{1/4}$ time dependence for interface-state generation. The generation of these field-sensitive interface states is thermally activated with a field-dependent activation energy.

PACS numbers: 73.40.Qv

The generation of interface states in metal oxide semiconductor (MOS) devices resulting from bias stressing or irradiation has been the subject of extensive investigation over many years. Increases in the number of interface states with time have been reported for bias temperature stressing,[1,2] for exposure to ionizing radiation,[3–5] and for charge injection.[6–8] Winokur *et al.*[9] have studied the field and time dependence of the buildup of these interface states. Recently, McLean[10] has assembled many of these findings in an empirical model describing the behavior of radiation-induced interface states in SiO_2 MOS structures. This body of knowledge underscores the importance of the radiation behavior of MOS devices in systems requiring hardened microelectronic circuits. One feature of the studies cited is that all are concerned with the permanent increase in interface states brought about by some environmental stress. Although much has been learned about the generation of interface states and physical models have been proposed, the radiation response of MOS oxides still cannot be predicted in a nondestructive manner.

We have observed the generation of interface states in SiO_2 MOS capacitors that are field and time dependent as well as thermally activated. The distinction between our work and the previous work is that the states are not permanent and will anneal out in short times (2 min) at room temperature. A strong correlation has been found between these metastable interface states and the radiation hardness of the MOS devices. The interface states are created by the application of an electric field, typically at room temperature. The number of states is determined from the difference between C-V curves measured at 77 K before and after application of the field. The number of states generated by the electric field is dependent on the magnitude and direction of the electric field, the length of time it is applied, and the temperature at which it is applied. This effect has been observed on a variety of samples with different processing histories.

The number of interface states created by the application of the field at room temperature can be calculated by measuring the difference in voltage V at a given capacitance between the polarized an unpolarized C-V curves measured at low temperature. The number of interface states is given by $N_{it} = C_{ox} V/e$,[7] where C_{ox} is the insulator capacitance per unit area and e is the electronic charge.

For the polarized C-V curve, the sample is biased at room temperature and then cooled to a low temperature with the bias maintained. Figure 1 compares the C-V curves at 125 K of an unpolarized capacitor to those of samples which were positively and negatively polarized, respectively, with fields of plus (+) and minus (−) 4×10^6 V/cm. The voltage sweep rate was 16 mV/s and the frequency was 15 kHz. No hysteresis was observed in the C-V measurements at 125 K under these conditions. For the positively biased capacitor the C-V curve is identical whether measured from accumulation to depletion or vice versa. For the negatively biased n-type capacitor, the sample must be maintained in inversion, and the measurement made from inversion to accumulation for an effect to be observed. Once the negatively biased sample has reached accumulation, subsequent measurement shows the curve to be identical to the unbiased C-V curve. Inversion of the negatively biased capacitor by optical illumination at 125 K does not reproduce the original effects. The results reported in this letter deal with the effects of positive polorization. The change in the C-V curve for positive polarization is attributed to the introduction of field sensitive interface states rather than charged lateral nonuniformities, based on the experimentally observed frequency dependence of the distortion to the C-V characteristics. As shown, the number of surface states induced by the field is quite large, i.e., $N_{it} = 2\times10^{12}$ cm^{-2} at flat band.

Samples used in this study consisted of aluminum-gate MOS capacitors with a thermally grown wet-gate oxide, 750 Å thick on 8-Ω cm, n-type, ⟨111⟩ silicon. Gate oxidation

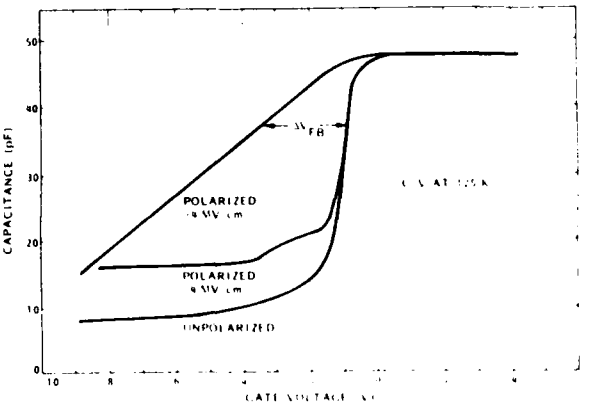

FIG. 1. Effect of room-temperature polarization (± 4 MV/cm, 10 min) on the low-temperature C-V characteristic of a MOS capacitor

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was performed at 1000 °C followed by a 20-min anneal in N_2 at 1000 °C. Five wafers were processed simultaneously, except for the additional postoxidation anneal shown in Fig. 2. The aluminum was *e*-beam evaporated and sintered at 475 °C. (Bias-stress temperature measurements consisting of 1 MV/cm at 250 °C showed that mobile ion contamination was negligible.) The anneals listed in Fig. 2 were chosen because they had been shown to affect the radiation hardness of the oxide.[11] The area of the capacitors was 1.03×10^{-3} cm^2. When this procedure was completed, there was no observable systematic difference between capacitors from any of the five wafers based on standard high-frequency, room-temperature *C-V* measurements. However, when the amount of field-induced interface states was measured following a 4-MV/cm bias for 10 min at room temperature, a dramatic wafer-to-wafer variation was observed. As shown in Fig. 2, the magnitude of the field-sensitive interface-state charge measured at flat band varied by a factor of 30 as a result of the different anneals.

After characterization of the field-sensitive interface states, the capacitors were irradiated with a Co^{60} γ source to a total dose of 5×10^5 rads (Si). Following irradiation, the flat-band voltage shifts of the capacitors were measured at increasing intervals of time. In Fig. 2 the average flat-band voltage shift $\Delta\overline{V}_{FB}$ for capacitors irradiated under zero bias (open circuit) and measured 45 days after exposure, is compared to the average preirradiation field-sensitive interface-state charge $\overline{Q}_{it}=C_x\Delta V$ obtained from positive bias experiments. The functional relationship between the two quantities appears to be exponential; qualitatively, therefore, we can predict which wafers, prior to exposure to ionizing radiation, will be harder than others.

The number of interface states created by the application of the electric field has been found to be linearly dependent on the magnitude of the applied field. Figure 3(a) shows

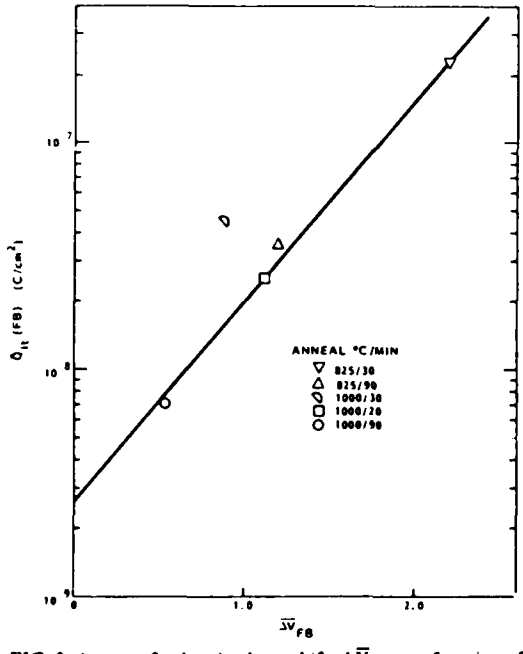

FIG. 2. Average flat-band voltage shift, $\Delta\overline{V}_{FB}$, as a function of the average preirradiation field-sensitive charge Q_{it}.

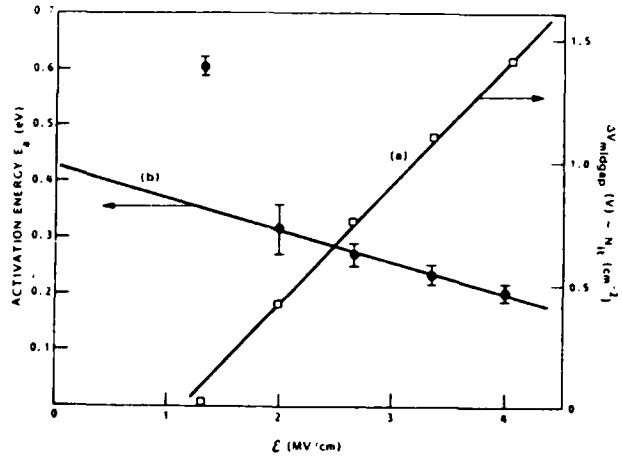

FIG. 3. (a) Magnitude of the field-sensitive interface states generated under positive bias at room temperature for 10 min as a function of the applied field. (b) Activation energy for generation of the field-sensitive interface states under positive bias as a function of the applied field.

the difference in voltage at midband between the polarized and unpolarized capacitor as a function of the applied field $\mathcal{E}$(MV/cm). The quantity ΔV_{midgap} is directly proportional to N_{it} at midgap. The sample was polarized at the indicated field for 10 min at room temperature. The data indicate that there is a threshold field for the appearance of the interface states of approximately 1 MV/cm.

Figure 4 shows the time dependence for the creation of the field-sensitive surface states. The capacitor was polarized at room temperature with a field of 4 MV/cm for varying times. It was then lowered to 90-K temperature, and the difference between polarized and unpolarized *C-V* curves measured. As seen in the figure, there is a $t^{1/4}$ dependence for the field-induced generation of interface states. Jeppson and Svensson[2] have likewise reported a $t^{1/4}$ behavior for the generation of interface states by negative bias stressing. They suggest that the $t^{1/4}$ behavior indicates a two-step diffusion-controlled process.

In addition to the field and time dependence for the creation of field-sensitive interface states, there is a temperature dependence. The number of interface states created as a function of the temperature at which the electric field is applied for a given field and polarization time has been found to follow a simple Arrheneus relation.

$$N_{it}(T)=N_0e^{-E_A/kT},$$

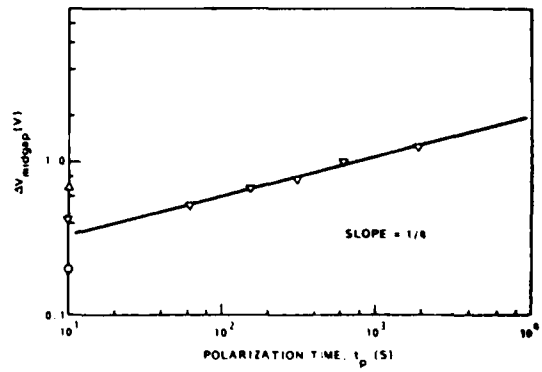

FIG. 4. Time dependence for creation of field-sensitive surface states.

where $N_{it}(T)$ is the number of interface states created at the polarization temperature T, N_0 is the preexponential constant, and E_A is the activation energy for formation of the interface states.

This relationship has been found to fit the data over a wide range of polarization temperatures ($-$ 20–100 °C) and applied fields (1–4 MV/cm). The activation energy for interface-state generation as a function of the applied electric field is also shown in Fig. 3(b). The data show that the activation energy for field-sensitive interface states is itself field dependent.

Except for the activation energy at a field of 1.33 MV/cm, which is very close to the threshold field in the curve on field dependence, the data in Fig. 3(b) can be fit by a straight line. The expression for a field-assisted activation energy is

$$E_A = E_0 - qd\varepsilon/2,$$

where E_0 is the zero field activation energy, d is the reaction coordinate describing the distance over which the process being described is taking place, and ε is the applied electric field. Applying this equation to the data in Fig. 4, we find a zero-field activation of 0.42 eV and a reaction of coordinate of approximate 1.4 nm.

As shown in Fig. 1, the effect of a negative bias on the formation of field-sensitive interface states is substantially different from that of a positive bias. If the capacitor is maintained in inversion and the C-V curve measured from inversion to depletion, a sharp bump, in contrast to the stretchout seen for positive-bias, appears in the capacitance curve. This sharp bump is seen only on the initial measurement from inversion to depletion. Reestablishing inversion by shining light on the capacitor while in deep depletion and then measuring the C-V curve give results identical to those of the unpolarized C-V curve. Also, maintaining the device in inversion with $-$ 4 MV/cm applied at 125 K for more than 1 h will not reestablish the effect. In contrast to the linear field dependence for the positively biased case, the number of field-sensitive interface states induced with negative voltage has an $\varepsilon^{1/2}$ field dependence.

Work on the investigation of the field-sensitive interface states and their role in the radiation response of MOS devices is continuing.

We would like to thank Dr. W. W. Anderson for valuable discussions and suggestions. This work was supproted by the Independent Research Fund of Lockheed Missiles and Space Company, Inc.

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APPENDIX B

A MODEL FOR FIELD-SENSITIVE INTERFACE STATES

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Oxygen derived point defects called Intimate-Valence-Alternation-Pairs (IVAP) appear to be able to account for the time, temperature, and field dependence of the generation of field-sensitive interface states. The theory and properties of IVAP defects in SiO_2 are described. A model for the observed changes in the capacitance voltage characteristics of Metal-Oxide-Semiconductor structures based on the existence of these defects is proposed. Finally the model is compared to existing data from the literature on the buildup of interface states caused by charge injection or ionizing radiation.

PACS numbers: 73.40.Qv, 71.55.Jv

I. INTRODUCTION

We recently reported[1] on the generation of interface states in SiO_2 metal oxide semiconductor (MOS) capacitors that are field and time dependent, as well as thermally activated. The unique feature of our observations is that the interface states generated are not permanent and will anneal out in short times (< 2 min) at room temperature. A strong correlation has been found between these metastable interface states and the radiation hardness of the MOS devices. We present in this paper a model of candidate defects whose physical and electronic properties are consistent with parameters observed in the field sensitive interface states.

This model is known as the Valence Alternation Pair (VAP) model. Originally proposed by Street and Mott[2] and later refined by Kastner, Adler, and Fritzsche,[3] this model provides a natural microscopic framework for a bipolar type defect composed of two oppositely charged oxygen derived species that are associated with intrinsic bonding defects in the oxide. First applied to localized diamagnetic states in the gap of amorphous chalcogenides, the VAP model, or rather a suitably modified version thereof, was extended to a-SiO_2 by Lucovsky[4,5] and Mott.[6] In this paper we advance the claim that the C-V measurements can and do provide additional support for the existence of oxygen-derived VAP type defects throughout the bulk of a-SiO_2 as well as at the silicon interface.

II. EXPERIMENTAL TECHNIQUES AND RESULTS

The field-sensitive interface states are created by the application of an electric field, typically at room temperature. The number of states is determined from the difference between C-V curves measured at 77 K before and after application of the field. The number of states generated by the electric field is dependent on the magnitude and direction of the electric field, the length of time it is applied, and the temperature at which it is applied. This effect has been observed on a variety of samples with different processing histories.

The number of interface states created by the application of the field at room temperature can be calculated by measuring the difference in voltage ΔV at a given capacitance between the polarized and unpolarized C-V curves measured at low temperature. The number of interface states is given by $N_{it} = C_{ox}\Delta V/e$,[7] where C_{ox} is the insulator capacitance per unit area and e is the electronic charge.

Low temperature, high frequency C-V curves of a MOS capacitor that are typical of those obtained from the first series of devices studied are shown in Fig. 1. The detailed processing history of these devices has been reported in Ref. 1. The curve labeled "unpolarized" is the deep depletion curve one obtains by making the C-V measurement at a low enough temperature (in this case 125 K) such that the thermogeneration rate of minority carriers is insufficient to form an inversion layer during the time of the measurement. It is to this curve that we will compare subsequent C-V curves. The curve labeled polarized $+4$ MV/cm was obtained after the sample had an electric field of $+4$ MV/cm (positive with respect to the gate) applied at 300 K for 10 minutes. The sample was rapidly cooled to 125 K with the field applied. The field was then removed, and the C-V characteristics determined. The low temperature C-V characteristics exhibited no hysteresis; i.e., the C-V curve was identical whether measured from accumulation to depletion or vice versa, regardless of how many times the measurement was made. If, however, the sample was warmed to 300 K and kept at this temperature for only a few minutes (~ 2 min), then returned to 125 K, the original "unpolarized" low temperature C-V characteristics were again observed. We interpret the distortion in the C-V curve to be due to the creation of metastable interface states by the applied electric field. We base our interpretation on several observations: (1) high temperature-bias stress of the capacitors showed that there was no mobile ionic charge in the oxide; (2) the distortion of the low temperature polarized C-V curve displayed a frequency dispersion; and (3) the phenomenon is reversible and is not permanent at room temperature.

It is noted that the positively polarized curve displays a distortion that is indicative of interface traps near midgap that are in communication with the silicon. However, we would expect that for interface traps with capture cross sections of the order of 10^{-15} cm^2, obeying Shockley-Read-Hall recombination statistics, the change in traps near midgap will be frozen in during the time of measurement. This apparent contradiction, while not resolved at this point, does not conflict with the proposed model. An explanation may be sought in a more complicated trapping and emission process than the simple Shockley-Read-Hall model or in assum-

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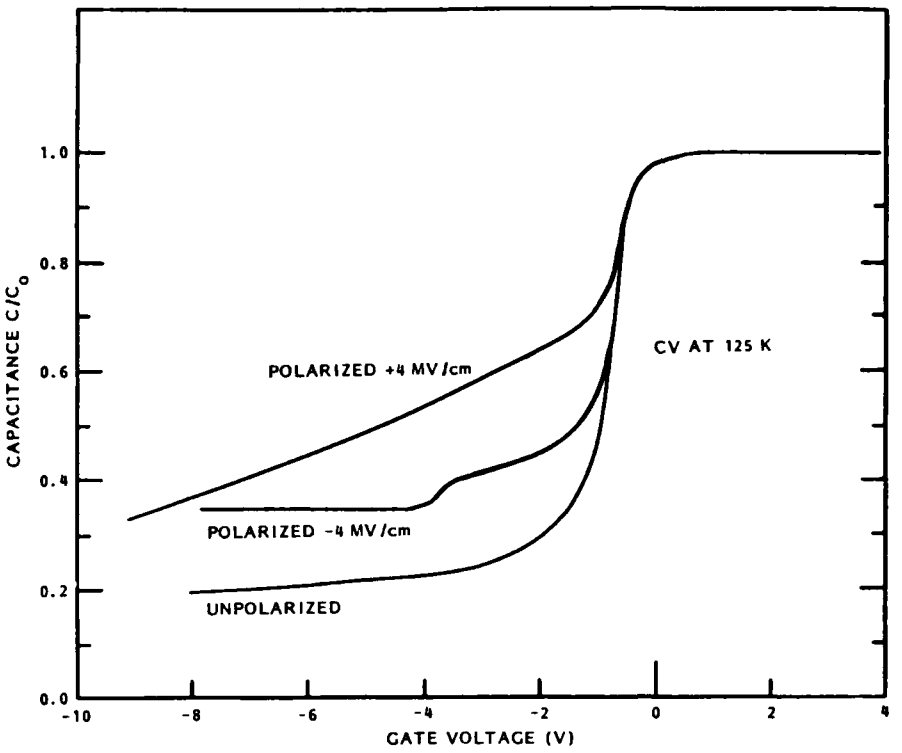

FIG. 1. Effect of room temperature polarization ($\pm$ 4 MV/cm, 10 mn) on low temperature C-V characteristic of a LMSC MOS capacitor (C_0 = 47 pf).

ing that the metastable defects are themselves distributed in a spatially nonuniform manner similar to the laterally nonuniform (LNU) distribution of charge as discussed by Zamani and Maserjian.[8] Both interpretations can be accommodated within the proposed model as discussed in Sec. IV.

The curve labeled "Polarized $-$ 4 MV/cm" in Fig. 1 represents the same sample after $-$ 4 MV/cm has been applied at 300 K for 10 min and measured at 125 K. It is a peculiarity of this first series of samples that the distortion of the C-V curve for negative bias could only be observed if the

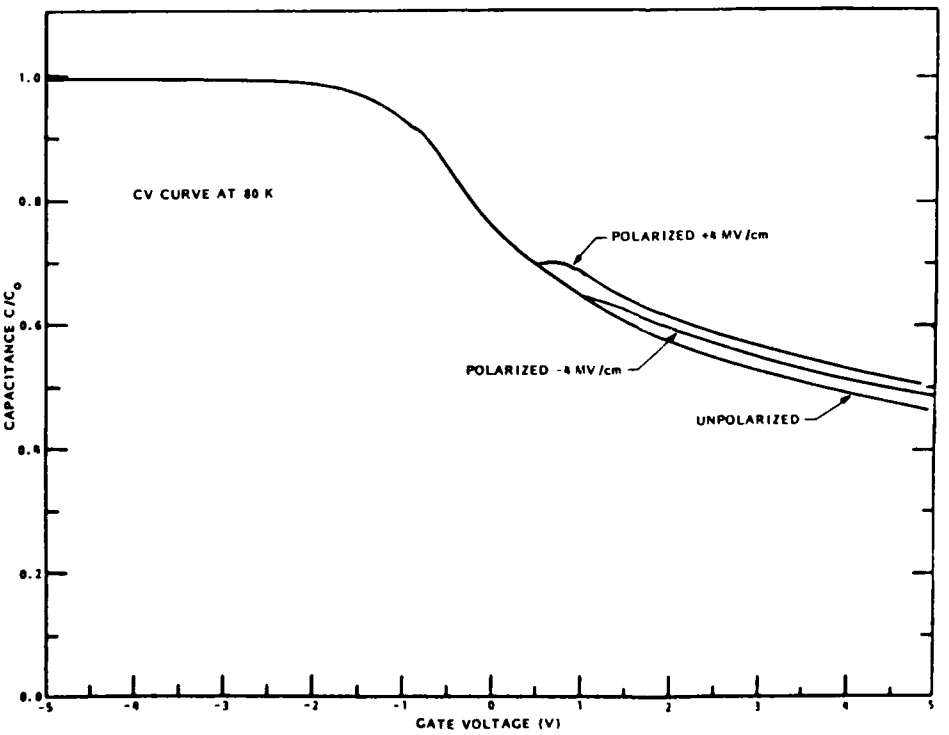

FIG. 2. Effect or room temperature polarization (+ 4 MV/cm, 30 minutes) on low temperature C-V characteristic of a RCA MOS capacitor (C_0 = 21 pf).

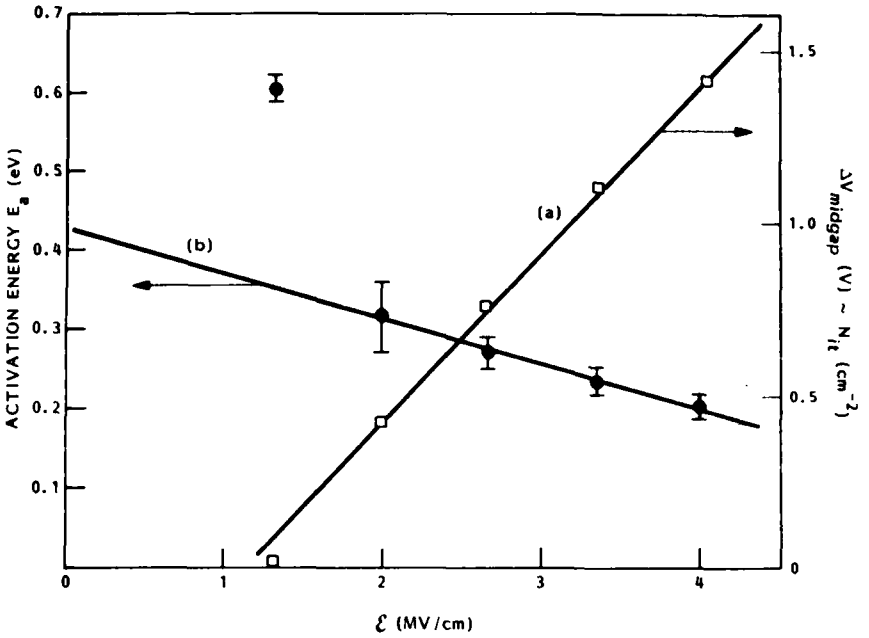

FIG. 3. (a) Magnitude of the field-sensitive interface states generated under positive bias at room temperature for 10 min as a function of the applied field. (b) Activation energy for generation of field sensitive interface states under positive bias as a function of the applied field.

sample was maintained in inversion upon cooling and the gate-voltage varied from inversion to accumulation. Subsequent measurement from accumulation to inversion and back retraced the unbiased curve. The field induced distortion in the C-V curve for negative bias could be restored by repolarizing at elevated (300 K) temperature. This, however, was not the case for a series of MOS capacitors manufactured by RCA. A typical result for a p-type MOS capacitor is drawn in Fig. 2. Here the curves for both positive and negative biases display the retraceability as discussed previously for the positive bias in the first series of devices. The fact that the low temperature measurements for the RCA devices were performed at 80 K, not 125 K, may have some bearing on the difference in characteristics between the two sets. The positive biased RCA sample also shows a pronounced ledge in the C-V curve as opposed to the stretchout seen in the first series of capacitors. The interface states introduced in the RCA sample are, however, similarly metastable, annealing out as the sample is returned to room temperature.

The most complete characterization of field sensitive interface states has been carried out for n-type MOS capacitors polarized with a voltage positive with respect to the gate.

The number of interface states created by the application of the electric field is linearly dependent on the magnitude of the applied field. Figure 3(a) shows the difference in voltage at midband between the polarized and unpolarized capacitor as a function of the applied field $\mathcal{E}$(MV/cm). The quantity ΔV_{midgap} is directly proportional to N_{it} at midgap. The sample was polarized at the indicated field for 10 min at room temperature. The data indicate that there is a threshold field for the appearance of the interface states of approximately 1 MV/cm.

Figure 4 shows the time dependence for the creation of the field sensitive surface states. The capacitor was polarized at room temperature with a field of 4 MV/cm for varying times. It was then lowered to 90 K temperature, and the difference between polarized and unpolarized C-V curves measured. As seen in the figure, there is a $t^{1/4}$ dependence for the field-induced generation of interface states.

In addition to the field and time dependence for the creation of field-sensitive interface states, there is a temperature dependence. The number of interface states created as a function of the temperature at which the electric field is applied for a given field and polarization time has been found to follow a simple Arrhenius relation:

$$N_{it}(T) = N_0 e^{-E_A/kt}, \tag{1}$$

where $N_{it}(T)$ is the number of interface states created at the polarization temperature T, N_0 is the preexponential constant, and E_A is the activation energy for formation of the interface states.

This relationship has been found to fit the data over a wide range of polarization temperatures ($-$ 20–100 °C) and applied fields (1–4 MV/cm). The activation energy for interface-state generation as a function of the applied electric

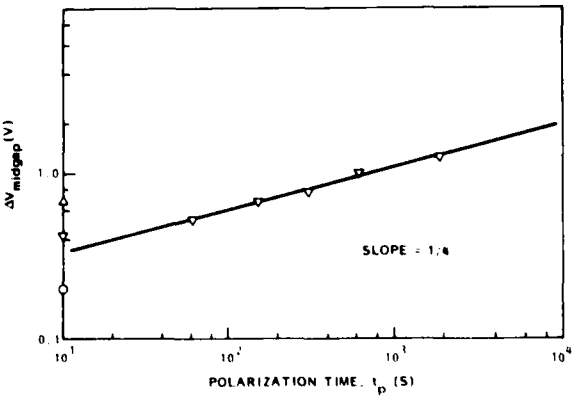

FIG. 4. Time dependence for creation of field-sensitive interface states.

field is also shown in Fig. 3(b). The data show that the activation energy for field-sensitive interface states is itself field dependent.

Except for the activation energy at a field of 1.33 MV/cm, which is very close to the threshold field in the curve on field dependence, the data in Fig. 3(b) can be fit by a straight line. The expression for the field-assisted activation energy is

$$E_A = E_0 - qd\mathscr{E}/2, \tag{2}$$

where E_0 is the zero field activation energy, d is the reaction coordinate describing the distance over which the process being described is taking place, and $\mathscr{E}$ is the applied electric field. Applying this equation to the data in Fig. 3(b) we find a zero-field activation of 0.42 eV and a reaction coordinate of approximately 1.4 nm.

For the same experimental conditions of field, temperature and time amount of field sensitive interface states is highly dependent on process. For example, a change of 175 °C in the post oxidation anneal can change the density of metastable defects by more than a factor of 30.

Characterization of the field sensitive interface states for n-type MOS capacitors polarized with voltage negative with respect to the gate is not as complete at this time. However, it has been observed that the response is not symmetric with respect to the energy distribution of the induced interface states for positive and negative polarizations. And secondly, the number of field sensitive interface states displays a power law dependence on the applied electric field; i.e., $N_{it} \propto \mathscr{E}^{1/2}$ at lower applied fields (<2 MV/cm) going to $N_{it} \propto \mathscr{E}^2$ at higher applied fields (>2 MV/cm).

In order to explain all the observed phenomena, we need a defect which is capable of producing the observed interface state energy levels, consistent with the field, time and temperature dependencies described, yet is neutral in the unbiased state. Such a defect can be found in a class of defects known as valence alternation pairs (VAP).

Since some of the details of the VAP model are crucial to subsequent comparisons with data, a brief review of the model is now presented.

III. THE VALENCE ALTERNATION PAIR (VAP) MODEL

Derived from dangling chalcogen bands (denoted by D^0 using the notation of Street and Mott), a charged pair defect consisting of over and under coordinated chalcogen atoms (designated as D^+ and D^-, respectively) forms as the lowest energy ground state whenever the reaction

$$2D^0 \rightarrow D^+ + D^- \tag{3}$$

is exothermic. The energy required to form a (singly coordinated) D^- is assumed to be overcompensated by the deformation energy released when a D^+ forms an extra bond with a neighboring chain (thus becoming triply coordinated). The ability of chalcogen atoms to participate in such a bonding configuration is predicated by the presence of the normally nonbonding lone pair electrons characteristic of group VI elements. The relative energies of the various bonding configurations have been delineated by Kastner, Adler, and Fritzsche[3] in the context of an elementary chemical bonding model and used to demonstrate that such a charged pair is indeed likely to be the lowest energy defect in chalcogenide amorphous semiconductors such as a-Se and in arsenic chalcogenide such as a-As_2Se_3. Since D^+ and D^- contain no unpaired electrons, the model provides a natural explanation for the absence of an ESR signal in such compounds at thermal equilibrium, and is in accord with luminescence and trap limited transport data as well.

An important property of the defects is embodied in the so-called interconversion reactions which provide the dominant mechanism for trapping holes and/or electrons at the defect sites:

$$\begin{aligned} D^- + 2h &\rightleftarrows D^+, \\ D^+ + 2e &\rightleftarrows D^-. \end{aligned} \tag{4}$$

A negative correlation energy results whenever these interconversions are energetically favored, meaning that the reaction Eq. (3) is indeed exothermic (another way of stating this point is that the energy to add a second hole to D^- requires less energy than the first).

Ionicity effects and/or bonding constraints may have considerable import in determining whether the interconversion reactions Eq. (4) take place in specific compounds assuming that charged defects were quenched from the melt in the first place.

Thus, as pointed out by Lucovsky[5] and by Street and Lucovsky,[9] in a strongly ionic compound such as v-SiO_2, the reaction in Eq. (3) is likely to be endothermic as a result of the interchange [Eq. (4)] being energetically unfavorable. This, in turn, is a consequence of the much higher strength of the heteropolar Si-O bond as compared with the homopolar O-O and Si-Si bonds on the one hand, and the fact than a Si atom, being a group IV element cannot become fivefold coordinated on the other. Thus, D^+ and D^- are still the lowest energy defects because they preserve the total number of Si-O bonds, but upon thermal or optical excitations, they behave in a more complex way as compared with the same defects in amorphous chalcogenides. As Street and Lucovsky have suggested, there is now more than one neutral defect and several possible charged species as a consequence of interchange reactions such as

$$\begin{aligned} D^- + 2h &\leftrightarrows A^+, \\ D^+ + 2e &\leftrightarrows B^-, \end{aligned} \tag{5}$$

where A^+ and B^- represent some new charged defects. The primary experimental evidence cited by Lucovsky to support the existence of VAP defects in v-SiO_2 derives from IR and Raman Spectroscopic data. These are consistent with a density of VAP defects of the order of 10^{19} cm^{-3} and average defect center separation of 2–3 nm. The model is also consistent with the trap-limited transport properties of both minority and majority carriers subject to the stipulation that the two defect members are closely correlated in the random network. Such near neighbor VAP's have been dubbed Intimate-Valence-Alternation-Pairs (IVAP's) by Kastner, Adler, and Fritzsche.[3] Figure 5 shows a possible local atomic configuration of an IVAP defect. Other configurations may have both defect members bonded to the same silicon atom. We note that IVAP's are expected to behave effectively as

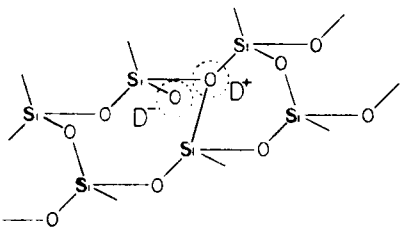

FIG. 5. Local atomic configuration of possible IVAP defect for a case when the two defect members are bonded to different silicon atoms.

neutral scattering centers as long as the pair separation is comparable to interatomic distance.

It has also been suggested that IVAP centers are associated with the ESR signals produced by E' and oxygen hole centers in irradiated v-SiO_2.[10] The basic argument is that the photogenerated electrons and holes get trapped in the charged defect centers producing two types of neutral defects that are stable against a second reconstruction. The Q_{II} defects found in the Si-SiO_2 interface may have their physical origin in similar processes. Since these are fixed positive changes physically located in the oxide, it is tempting to associate them with isolated D^+ centers as Lucovsky has recently advocated.[11] This would require postulating an excess D^+ over D^- centers, not too unreasonable an assumption in view of the departures from pure stoichiometry that occur near the interface. Thus, a silicon rich transition region may lead not only to a high concentration of Si-Si bonds (and to trivalent silicon) but also to the formation of D^+ centers that can bond to three silicon neighbors. Since large negative relaxation energies accompany the formation of the extra bond, an overabundance of D^+ defects (over their D^- partners) can be expected.

IV. FIELD SENSITIVE INTERFACE STATES AND THE IVAP MODEL

As we will now proceed to show, field generated interface states can be understood as a natural consequence of oxygen derived VAP defects subject to the following stipulations: (1) Oppositely charged oxygen centers (denoted D^+ and D^-) exist throughout the bulk of the oxide as well as at the interface region in the form of near-neighbor pairs, i.e., IVAPs. In this form, the defect is neutral, and we assume that it has no energy levels within the silicon band gap. (2) When pulled sufficiently apart, both D^+ and D^- states have an energy distribution in the oxide band gap such that a substantial fraction of localized levels is found in the silicon band gap. The positive donor states are located primarily in the upper half of the gap and the negative acceptors in the lower half.

The first assumption is consistent with most data on SiO_2 as mentioned in the previous section as well as with the fact these interface states are not observed under normal conditions. The second assumption is also reasonable enough in view of expected variations in the chemical bond parameters such as bondlengths and bond angles.[12] Such variations may indeed give rise to states which are continuously distributed in energy.[13] This assumption is also compatible with the recently proposed model of band tail states induced by the presence of thin, disordered semiconductor layer at the interface.[14] Such a layer may be responsible for the often-observed U-shaped density of interface states versus energy curves,[15] on top of which highly localized defects, such as the ones considered in this paper induce additional specific structure. One may also invoke the idea of scattering-induced band tails[16] in order to simulate interface-state-like behavior for those states that conform to the first assumption but which are located outside the silicon band gap, thereby relaxing the requirement imposed by assumption (2). The detailed incorporation of this idea in the model represents an interesting possible extention of the model. It lies, however, beyond the scope of the simple qualitative analysis presented in this work and will not be mentioned further. In any case, the tendency for D^+ states (D^- states) to be concentrated in the upper (lower) half of the gap is maintained in our formulation in accordance with previous molecular bonding orbital assignments for the charged defects and their relation to bond orbital structure.

The metastable nature of the field generated interface states can now be naturally attributed to the fact that an IVAP behaves essentially as a neutral scattering center in the absence of a field [cf. assumption (1)]. Upon the application of a field, the charged members of the pair are separated, and the appropriate charged defect (the charge determined by the bias polarity) diffuses toward the interface, probably via some bond hopping mechanisms. The pair relaxes back to its initial bipolar state when the field is removed and the sample is allowed to stand at room temperature. This explanation accords well with the observed linear field dependence and the $t^{1/4}$ behavior as is expected in a two-step diffusion controlled process.[17] At higher fields, contributions from Fowler-Nordheim tunneling emission from the Si substrate into the oxide may modify both field and time dependencies. The appearance of an $\mathscr{E}^2$ dependence is thus not unlikely (a Fowler-Nordheim type mechanism may be similarly linked with charge buildup introduced into the oxide by high-field stressing as suggested recently.[18] A similar mechanism has also been proposed by Kirk[19] to account for fatigue and positive charge build-up effects in NMOS memory devices). We note here that the metastable nature of the observed interface states can be explained without invoking a particularly large number of bulk oxide defects. An adequate interpretation of the data would involve primarily those states which are located within some distance l from the interface as long as l is larger than one or two atomic layers.[20] In this case, increasing the field still leads to increased separation of the charged defect members that is sufficient for the electronic states to move from within the bands into the band gap.[13] The displacement is frozen in at liquid nitrogen temperatures to give the interface state. In this case, however, more detailed considerations are required in order to account for the diffusion-like characteristics of the data at low fields, a difficulty which is alleviated if some contribution from bulk defect pairs is assumed (i.e., large enough l).

Referring now to Fig. 1, the shape of the observed C-V curves can be understood from the behavior of the charged defect that has diffused towards the interface. This defect can now exchange charge with the semiconductor provided

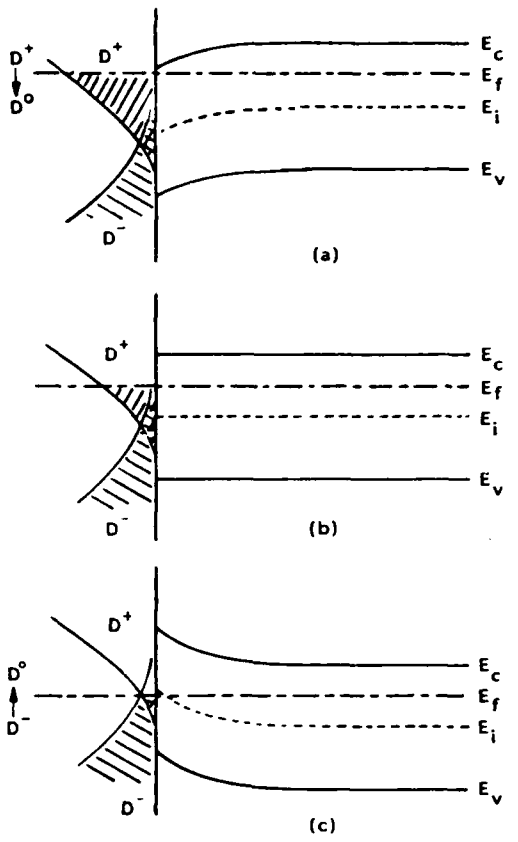

FIG. 6. Energy band diagram for an *n*-type MOS structure under conditions of (a) accumulation, (b) flat band, and (c) inversion. The illustrated energy distribution for IVAP defects near the interface displays a minimum near midgap but is otherwise arbitrary.

its energy places it within the Si band gap. According to assumption (2), a substantial number of both defect members may fulfill this condition.

Figure 6 indicates the energy band diagram in a MOS system at thermal equilibrium in accumulation, flat band, and inversion conditions. The energy distribution assumed for the charged defects displays a minimum near midgap in accordance with theoretical expectations (as well as with some experimental data[15]). The distribution is otherwise arbitrary (although, for simplicity we show it increasing gradually towards the band edges).

For positive bias, the deep depletion curve in Fig. 1 can be understood with the help of the model as follows: Positive bias means that it is the Positive D^+ states that migrate to the interface. At accumulation, those states that are below the Fermi level have captured an electron from the Si conduction band to become the singly occupied D^0 states (see Fig. 6). Sweeping the gate voltage from accumulation to depletion changes the position of the Fermi level relative to the intrinsic level at the interface and alters the occupation of these trapping states. This explanation accounts for the stretchout manifested by the positive bias curve in Fig. 1, provided that either (a) carriers are not frozen in the interface states even at energy levels below 0.29 eV from the conduction band or (b) if carriers are frozen in the interface states there is a laterally nonuniform distribution of such states. In either case, varying the voltage back towards positive values should retrace the original curve (at least to within experimental resolution limits).

For negative bias, the D^- states are the ones swept towards the interface. These states are expected to exhibit a similar behavior towards carrier capture and release as their D^+ counterparts except that minority carriers are now being captured. At inversion those D^- states that were above the Fermi level have captured a hole to become D^0 states (Fig. 6). Sweeping the bias towards accumulation should result in some of the captured carriers being released into the silicon valence band (except, again, for those states that are more than 0.29 eV from the valence band edge and may have frozen in carriers as noted for the positive bias case). The negative curve in Fig. 1 indicates indeed that such a process may be taking place. However, sweeping the bias back down towards depletion does not reproduce the curve. Instead, the curve obtained resembles the zero bias curve.

There are two points of asymmetry between the positive and negative bias behavior of the interface states as shown in Fig. 1, i.e., a stretchout of the *C-V* curve vs a ledge and the nonretraceability of the negative biased curve. This would seem to imply some inherent difference in the role of the positively charged center as compared with its negative counterpart. One possible explanation for the nonretraceability of the negative biased curve may be to invoke an overabundance of D^+ states near the interface. These may be related to the observed fixed charges Q_f and Q_{it} in the sense that both can be represented by uncompensated D^+ centers but with different energy levels. Only those D^+ states with energy appropriate for communication with the silicon surface charge distribution contribute to interface states. The others (those outside the silicon band gap), will manifest themselves as fixed charges and are field independent. The positively charged interface states, if in sufficient numbers near the interface, may indeed lead to the kind of asymmetric behavior observed experimentally. If this hypothesis is correct, we would, in fact, expect to see a correlation between the density of fixed oxide charges and manifestly asymmetric, bias dependent, *C-V* characteristics.

Our second set of samples also displayed the field induced interface state in *C-V* curves for both *n*-type and *p*-type, positive and negative bias. Differences between the two sets of samples are possibly due to the different processing technologies and oxidation conditions as well as the fact that they involve two different wafer orientations. Set 1 was grown on (111) silicon which is known to have higher concentrations of both interface states and fixed oxide charge than oxides grown on (100) silicon as in Set 2. More complete measurements of Set 2 are currently in progress which will hopefully shed more light on some of the details in the model, as well as establish a direct correlation of both interface state and oxide charges densities with process conditions.

In summary, while we believe that oxygen-derived defects such as IVAPs play an important role in the observed properties of MOS structures, the model is in all probability too simple to account for the full complexity of the interface on an atomic level. There is experimental evidence indicat-

ing that silicon and water related species exist as well, and these together with any impurities present in the material must be incorporated into any full treatment, especially if radiation effects are to be accounted for. Clearly, the model is not unique in the sense that other defects or impurities that can form charge pairs may exhibit properties that are similar to the ones inferred from the oxygen-derived defects. In fact, the present experimental evidence cannot establish the definite identity of the charges involved. A major argument for the preeminence of oxygen related charged defects can still be advanced, based on it being the lowest energy defect as compared with other possible species, though clearly more theoretical work is needed to categorically establish the validity of this argument, particularly near the interface. Other models such as the one considered by Breed[21] may account for some features of the data but cannot easily be reconciled with the experimental evidence taken in its entirety. The model discussed in this paper, on the other hand, while admittedly simple, accords rather well with all the gross features of the data. Furthermore, as we will show in the next section, the model, or suitable modifications thereof, is in good agreement with several other experimental results, and as a consequence, can be used in order to gain physical insight into some of the important questions concerning radiation effects on MOS devices.

V. DISCUSSION AND CONCLUSIONS

In this study we have shown that an oxygen-derived IVAP model is compatible with all the observed properties of field generated interface states. The model accounts qualitatively for the amphoteric nature of the generated surface states as well as their metastable nature as these are revealed by low-temperature C-V measurements. Plausible mechanisms have been suggested for the observed field, time and temperature dependence of interface buildup and anneal.

Additional evidence supporting the existence of charged pairs at the interface has been summarized and discussed by Pepper[22] based on device conductance measurements at liquid-nitrogen temperature. The IVAP model is compatible with his analysis as well as with data from recently reported low temperature electron photoinjection experiments.[23] The production of interface states by electron currents at moderate fields was interpreted as being due to pre-existing sites with densities of approximately 10^{12} cm^{-2} and interaction cross sections of 10^{-18}–10^{-19} cm^2 at 90 K. Such a low value for the cross section can be taken as indicative of neutral trapping center and is in accordance with the value assigned independently by Lucovsky[5] in connection with electron transport properties in silica. We are, therefore, led to stipulate a mechanism whereby electrons are captured by the D^+ member of the IVAP yielding a neutral D^0 which cannot undergo atomic rearrangement at the low-temperature conditions of the experiment. This leaves the negative (D^-) member of the original center free to exchange charge with the silicon and thereby become an interface state as manifested by the observed stretchout in the C-V curves. Naturally, we must assume that a sufficient number of IVAPs are located physically near the interface for the charge exchange process to take place at liquid nitrogen temperature. An interface state density of 10^{12} cm^{-2} inferred from the experiment accords rather well with the previously estimated density of IVAPs in the bulk (10^{19} cm^{-3}) if we assume that centers within 2 nm of the interface can interact with carriers in the Si bands. The observed annealing properties of the electron generated surface states in Ref. 13 are also compatible with the IVAP model, since at room temperature, gradual release of captured electrons is expected to be the dominant process, thereby leading to the experimentally observed behavior.

In addition to pre-existing IVAP defect pairs, newly created oxygen-derived centers may play a role in the observed generation of interface states under severe conditions such as high field stress or ionizing radiation. The experimental relation between high-field generated electron traps and interface states has been discussed in detail by Jenq.[24] Since his experiments involved subjecting the samples to field stress at 90 K (rather than at room temperature as we have done) local atomic rearrangements as well as dipole separation and/or reorientation must be ruled out. This means that pre-existing IVAP-type centers cannot give rise to interface states given the close proximity of the defect members. Nevertheless, the positive member of the pair can still act as an electron trap via the reaction $D^+ + e \rightarrow D^0$ just as pointed out above. Following internal e photoinjection, we should therefore observe some interface state density engendered by the uncompensated negative D^- member of the original defect. Such a behavior was indeed observed experimentally. The high field stress may, however, create additional dangling bonds—both oxygen and silicon derived. These may exchange an electron to yield a defect pair of the form $D^- - T^+$ where T denotes a silicon-derived defect. The positive T^+ can then act as an electron trap, leaving the uncompensated D^- to behave as an interface state even before the sample is warmed up. The high electron capture cross section observed in this particular experiment ($\sim 9 \times 10^{-14}$ cm^2) can be explained if we assume that the originally formed T^+ centers are sufficiently distant from their D^- counterparts for them to act essentially as Coulombic attractive defects. (Indeed, there is no reason to expect the defect pair formed under the specified experimental condition to be an IVAP.) Naturally, silicon derived defects such as T^0 (after e capture), and T^- (after two e capture) may also contribute to the observed interface state density and at the present there is no good way of distinguishing their effect from those of the oxygen-derived centers. It is also clear that if thermal energy is supplied to the MOS structure following the high field stress (with or without electron photoinjection), atomic rearrangements may alter the nature of the defects, thereby giving rise to another set of interface states. Such a behavior was indeed inferred from the data recorded in Ref. 24. A more detailed analysis of this experiment in light of our proposed interpretation is currently in progress.

Radiation-induced interface states such as the ones investigated by Mclean[25] also appear to be compatible with an oxygen-derived defect pair model, especially since the experimental evidence suggests a two-stage character for the interface state buildup. The first stage involves transport of radiation-generated holes through the oxide. The field de-

pendence suggests that the process may involve some interaction of the holes in which ionic charge is released. If we focus now on those pre-existing IVAP pairs, it is easy to envision a hole trapping process whereby the negative IVAP member captures holes via $D^- + h \rightarrow D^0$ (or even two holes via $D^- + 2h \rightarrow B^+$), thereby "releasing" the D^+ member of the defect. The second stage, which begins after the holes have reached the interface, involves the actual interface state buildup, a process which may continue for many minutes at room temperature. The interpretation given for this stage is that of a field-assisted ionic transport to the interface with a subsequent appearance of interface states. Furthermore, there is a polarity condition for the interface states to be observed. This then argues for a positively charged ionic specie which would drift toward the interface under positive bias. Evidently, the "liberated" D^+ member of the original IVAP pair matches these requirements, since it can migrate towards the Si interface by the same diffusion-controlled process we suggested earlier in the paper in connection with the appearance of field generated interface states. In fact, an average hopping distance of 2.6 Å found by Mclean on the basis of his empirical model agrees rather well with such a drift mechanism, since this value closely matches the average distance between nearest neighbor oxygen atoms in a SiO_2. The suggestion that negative D^- states are the hole traps observed upon irradiation has also been raised by Pepper,[22] who concludes that on the basis of the localization dependence of the slow states, it is most likely that the D^- centers close to the interface are the observed slow states. Naturally, a complete discussion of radiation-induced interface states should also include some contribution from possible silicon-derived defects which are present in irradiated silicon, as evidenced by ESR signals, as well as the effects of water-derived radicals. Although such a discussion transcends the scope of this paper, we hope to elaborate on it in a future publication. The primary goal motivating this paper was directed towards emphasizing the possibly important role of oxygen-derived centers, either alone or in pairs, in interface state buildup. We believe that sufficient evidence has been presented to warrant further, more detailed study of this class of defects.

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ATTN: S. Ives

Bell Labs
ATTN: D. Yaney
ATTN: R. McPartland

Boeing Aerospace Co
ATTN: M. Anaya, M/S 2A-87

Boeing Co
ATTN: D. Egelkrout
ATTN: H. Wicklein
ATTN: R. Caldwell
ATTN: 8K-38

Boeing Co
ATTN: C. Dixon
ATTN: MS-2R-00, A. Johnston
ATTN: MS-2R-00, C. Rosenberg
ATTN: MS-2R-00, E. Smith
ATTN: MS-2R-00, I. Arimura
ATTN: MS-81-36, P. Blakely
ATTN: MS-81-36, W. Doherty
ATTN: O. Mulkey

Booz-Allen & Hamilton, Inc
ATTN: R. Chrisner

California Institute of Technology
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ATTN: D. Nichols, T-1180
ATTN: F. Grunthaner
ATTN: J. Coss
ATTN: K. Martin
ATTN: P. Robinson
ATTN: R. Covey
ATTN: W. Price, MS-83-122
ATTN: W. Scott

Calspan Corp
ATTN: R. Thompson

Charles Stark Draper Lab, Inc
ATTN: A. Freeman
ATTN: J. Boyle
ATTN: N. Tibbetts
ATTN: P. Greiff
ATTN: R. Bedingfield
ATTN: R. Haltmaier
ATTN: R. Ledger
ATTN: Tech Library
ATTN: W. Callender

Cincinnati Electronics Corp
ATTN: L. Hammond

Clarkson College of Technology
ATTN: P. McNulty

Computer Sciences Corp
ATTN: A. Schiff

Control Data Corp
ATTN: D. Newberry, BRR 142

University of Denver
ATTN: Sec Officer for F. Venditti

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Develco, Inc
ATTN: G. Hoffman

Dikewood Corp
ATTN: Tech Lib for D. Pirio

E-Systems, Inc
ATTN: K. Reis

E-Systems, Inc
ATTN: Div Library

Eaton Corp
ATTN: A. Anthony
ATTN: R. Bryant

Electronic Industries Assoc
ATTN: J. Kinn

FMC Corp
ATTN: M. Pollock

Ford Aerospace & Communications Corp
ATTN: H. Linder
ATTN: Tech Info Svcs

Garrett Corp
ATTN: H. Weil

General Dynamics Corp
ATTN: O. Wood
ATTN: R. Fields, MZ 2839

General Electric Co
ATTN: D. Tasca
ATTN: J. Peden
ATTN: R. Benedict
ATTN: R. Casey
ATTN: Tech Info Ctr for L. Chasen
ATTN: Tech Library

General Electric Co
ATTN: B. Flaherty
ATTN: G. Bender
ATTN: L. Hauge

General Electric Co
ATTN: G. Gati, MD-E184

General Electric Co
ATTN: C. Hewison
ATTN: D. Cole

General Eelctric Co
ATTN: D. Pepin

General Research Corp
ATTN: A. Hunt

George Washington University
ATTN: A. Friedman

Georgia Institute of Technology
ATTN: Res & Sec Coord for H. Denny

Goodyear Aerospace Corp
ATTN: Security Control Station

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Grumman Aerospace Corp
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GTE Communications Products Corp
ATTN: H & V Group
ATTN: J. McElroy
ATTN: P. Fredrickson

GTE Communications Products Corp
ATTN: F. Krch

GTE Communications Products Corp
ATTN: J. Waldron
ATTN: M. Snow
ATTN: W. Dunnett

GTE Government Systems Corp
ATTN: L. Lesinski
ATTN: L. Pauplis

Harris Corp
ATTN: E. Yost
ATTN: W. Abare

Harris Corp
ATTN: B. Gingerich, MS-51-120
ATTN: C. Anderson
ATTN: D. Williams, MS-51-75
ATTN: J. Cornell
ATTN: J. Schroeder
ATTN: Mgr Linear Engineering
ATTN: Mngr Bipolar Digital Eng
ATTN: T. Sanders, MS-51-121

Honeywell, Inc
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ATTN: J. Moylan
ATTN: R. Gumm

Honeywell, Inc
ATTN: H. Noble
ATTN: J. Schaefer
ATTN: J. Zawacki
ATTN: MS 725-5
ATTN: R. Reinecke

Honeywell, Inc
ATTN: Tech Lib

Honeywell, Inc
ATTN: L. LaVoie

Honeywell, Inc
ATTN: D. Herold, MS-MN 17-2334
ATTN: D. Lamb, MS-MN 17-2334
ATTN: R. Belt, MS-MN 17-2334

Hughes Aircraft Co
ATTN: B. Campbell, E1/E110
ATTN: D. Binder
ATTN: R. McGowan

Hughes Aircraft Co
ATTN: R. Henderson

IBM Corp
ATTN: Electromagnetic Compatability
ATTN: H. Mathers
ATTN: Mono Memory Systems
ATTN: T. Martin

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Hughes Aircraft Co
ATTN: MS-A2408, J. Hall

Hughes Aircraft Intl Svc Co
ATTN: A. Narevsky, S32/C332
ATTN: D. Shumake
ATTN: E. Kubo
ATTN: W. Scott, S32/C332

IBM Corp
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IBM Corp
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ATTN: H. Kotecha
ATTN: L. Rockett, MS 110-020
ATTN: MS 110-036, F. Tietze
ATTN: N. Haddad
ATTN: O. Spencer
ATTN: W. Doughten
ATTN: W. Henley

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ATTN: I. Mindel
ATTN: R. Sutkowski

Illinois Computer Research, Inc
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Institute for Defense Analyses
ATTN: Tech Info Services

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ATTN: T. May

IRT Corp
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ATTN: MDC
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ATTN: Physics Div
ATTN: R. Mertz
ATTN: Systems Effects Div

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ATTN: R. Berger
ATTN: R. Stahl
ATTN: T. Flanagan

JAYCOR
ATTN: R. Sullivan

JAYCOR
ATTN: C. Rogers
ATTN: R. Poll

Johns Hopkins University
ATTN: P. Partridge
ATTN: R. Maurer

Johns Hopkins University
ATTN: G. Masson, Dept of Elec Engr

Kaman Sciences Corp
ATTN: E. Conrad

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ATTN: N. Beauchamp
ATTN: W. Rich

Kaman Tempo
ATTN: DASIAC
ATTN: R. Rutherford
ATTN: W. McNamara

Kaman Tempo
ATTN: DASIAC

Litton Systems, Inc
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ATTN: F. Motter

Lockheed Electronics Co, Inc
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Lockheed Georgia Co
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Lockheed Missiles & Space Co, Inc
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ATTN: J. Smith
ATTN: Reports Library
2 cys ATTN: L. Dries
2 cys ATTN: J. Crowley

Lockheed Missiles & Space Co, Inc
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ATTN: E. Hessee
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ATTN: J. Cayot
ATTN: L. Rossi
ATTN: P. Bene
ATTN: S. Taimuty

LTV Aerospace & Defense Company
ATTN: Library
ATTN: R. Tomme
ATTN: Tech Data Ctr

M I T Lincoln Lab
ATTN: P. McKenzie

Magnavox Advanced Products & Sys Co
ATTN: W. Hagemeier

Magnavox Govt & Indus Electronics Co
ATTN: W. Richeson

Martin Marietta Corp
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ATTN: J. Tanke
ATTN: J. Ward
ATTN: MP-163, W. Bruce
ATTN: R. Gaynor
ATTN: R. Yokomoto
ATTN: S. Bennett
ATTN: TIC/MP-30
ATTN: W. Brockett

Martin Marietta Corp
ATTN: T. Davis

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ATTN: P. Kase
ATTN: R. Anderson
ATTN: Research Library

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ATTN: H. Lin

McDonnell Douglas Corp
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ATTN: D. Dohm
ATTN: Library
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ATTN: R. Kloster
ATTN: T. Ender

McDonnell Douglas Corp
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ATTN: J. Imai
ATTN: M. Onoda
ATTN: M. Ralsten
ATTN: P. Albrecht
ATTN: P. Bretch
ATTN: R. Lothringer

McDonnell Douglas Corp
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George C. Messenger
ATTN: G. Messenger

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Mission Research Corp
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ATTN: D. Merewether
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Mission Research Corp
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ATTN: R. Curry
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Mission Research Corp, San Diego
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Mitre Corp
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Motorola, Inc
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National Semiconductor Corp
ATTN: F. Jones

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Norden Systems, Inc
ATTN: Tech Lib

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ATTN: J. Srour
ATTN: P. Eisenberg
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ATTN: Z. Shanfield

Northrop Corp
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ATTN: L. Apodaca
ATTN: P. Gardner
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ATTN: T. Jackson

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ATTN: H. Brode, Chairman SAGE

Palisades Inst for Rsch Services, Inc
ATTN: Secretary

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ATTN: J. Shea

Power Conversion Technology, Inc
ATTN: V. Fargo

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ATTN: P. Davis

Rand Corp
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Raytheon Co
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ATTN: J. Ciccio
ATTN: T. Wein

Ratheon Co
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ATTN: H. Flescher

RCA Corp
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ATTN: V. Mancino

RCA Corp
ATTN: Office N103
ATTN: R. Smeltzer

RCA Corp
ATTN: R. Killion

Research Triangle Institute
ATTN: M. Simons

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RCA Corp
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ATTN: L. DeBacker
ATTN: W. Allen

RCA Corp
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ATTN: R. Magyarics
ATTN: W. Heagerty

Rensselaer Polytechnic Institute
ATTN: R. Gutmann
ATTN: R. Ryan

Rockwell International Corp
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ATTN: J. Bell
ATTN: J. Blandford
ATTN: J. Burson
ATTN: J. Pickel, Code 031-BB01
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ATTN: R. Pancholy
ATTN: V. De Martino
ATTN: V. Strahan

Rockwell International Corp
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ATTN: TIC AJ01

Rockwell International Corp
ATTN: L. Pinkston, 106-183
ATTN: TIC 124-203

Rockwell International Corp
ATTN: T. Yates
ATTN: TIC BA08

Sanders Associates, Inc
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ATTN: D. Millward
ATTN: D. Strobel
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ATTN: J. Naber
ATTN: J. Retzler
ATTN: J. Spratt
ATTN: L. Scott
ATTN: R. Fitzwilson
ATTN: V. Orphan
ATTN: V. Verbinski

Science Applications Intl Corp
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ATTN: W. Chadsey

Science Applications, Inc
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Science Research Assoc, Inc
ATTN: H. Grubin

Singer Co
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ATTN: R. Spiegel
ATTN: Tech Info Ctr

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Signetics Corp
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Sperry Corp
ATTN: Engineering Lab

Sperry Corp
ATTN: J. Inda

Sperry Corp
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ATTN: F. Scaravaglione
ATTN: P. Maraffino
ATTN: R. Viola

Sperry Corp
ATTN: D. Schow

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ATTN: A. Whitson
ATTN: M. Tarrasch

SRI International
ATTN: A. Padgett

Sundstrand Corp
ATTN: C. White
ATTN: Rsch Dept

System Development Corp
ATTN: Product Eval Lab

Systron-Donner Corp
ATTN: J. Indelicato

Teledyne Brown Engineering
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ATTN: D. Guice

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ATTN: R. Suhrke

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ATTN: R. McGrath
ATTN: R. Stehlin
ATTN: T. Cheek, MS 3143

TRW Electronics & Defense Sector
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ATTN: D. Clement
ATTN: F. Friedt
ATTN: H. Holloway
ATTN: M. Ash
ATTN: P. Guilfoyle
ATTN: P. Reid, MS R6/2541
ATTN: R. Kingsland
ATTN: R. von Hatten
ATTN: Tech Info Ctr
ATTN: W. Adelman
ATTN: W. Rowan
ATTN: W. Willis
2 cys ATTN: O. Adams
2 cys ATTN: R. Plebuch, 134/8085, Hard & Surv Lab

TRW Electronics & Defense Sector
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ATTN: J. Gorman

Westinghouse Electric Corp
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ATTN: E. Vitek, MS 3200
ATTN: H. Kalapaca, MS 5155
ATTN: J. Cricchi
ATTN: L. McPherson, MS 484
ATTN: MS 3330
ATTN: N. Bluzer

Westinghouse Electric Corp
ATTN: S. Wood

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